
Open Source Chip Design panel

— 2021 Open Hardware Summit —

Megan Wachs, bunnie, Mohamed Kassem, Jason Kridner

Slides: <https://bit.ly/3dLVlhc>

Megan Wachs

- Megan Wachs currently serves as VP of Hardware Engineering at [SiFive](#), the company founded by the creators of the RISC-V ISA. She has helped bring the first commercial RISC-V silicon to market in the FE310 chip used in the [HiFive1](#) board. Megan has served the [RISC-V Foundation](#) as Chair for the Debug Task Group. Prior to joining SiFive as an early engineer, she designed and implemented secure cryptographic hardware at Rambus. Megan earned her Ph.D. in Electrical Engineering from Stanford University and her undergraduate degree in Engineering from Brown University. In her free time she swims in San Francisco Bay and chases her sons up and down San Francisco's hills.
- **RISC-V and FPGAs: Open Source Hardware Hacking**
 - [Hackaday Supercon 2019 keynote](#)
 - [Slides](#)



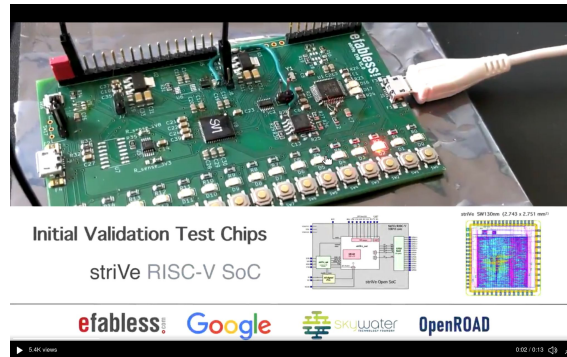
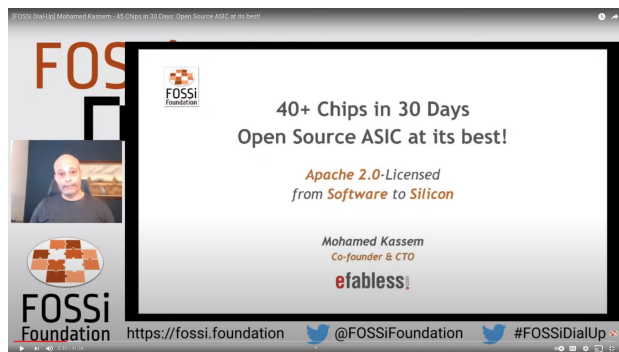
bunnie

- bunnie is best known for [hacking the Microsoft Xbox](#), as well as for his efforts in designing and manufacturing open source hardware, including the [chumby](#) (app-playing alarm clock), [chibitronics](#) (peel-and-stick electronics for craft), and the [Novena](#) DIY laptop. He received his PhD in EE from MIT in 2002. He currently lives in Singapore where he runs a private product design studio, [Kosagi](#), and he actively mentors several startups and students.
- **[Precursor](#): Open Hardware, RISC-V System-on-Chip Development Kit**
 - [Can We Build Trustable Hardware?](#)
 - Recent talk at [FOSS North](#)



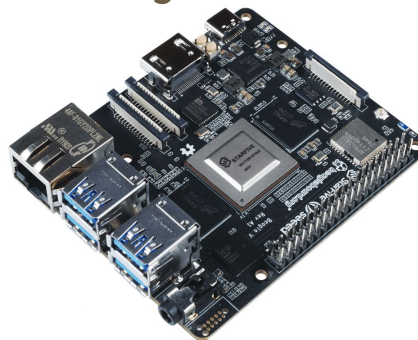
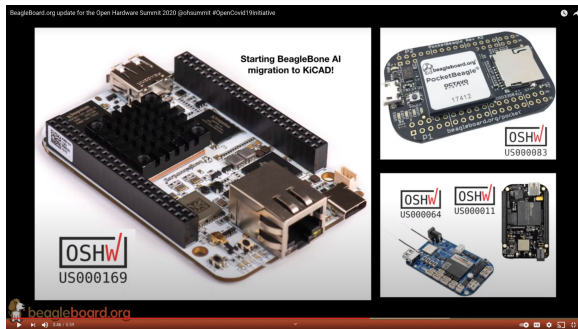
Mohamed Kassem

- Mohamed Kassem is the cofounder and CTO of [efabless corporation](https://efabless.com). The world's first community-centric hardware design company applying community expertise to all aspects of semiconductor product development. The company simplifies the process of developing smart hardware and opens it to anyone. Prior to launching efabless, Mohamed designed wireless application processors at Texas Instruments including the integration of major phone functions into a single SoC. Mohamed holds a Masters in Electrical Engineering from the University of Waterloo in Canada.
- [45 Chips in 30 Days: Open Source ASIC at its best!](#)
- [striVe 1: 100% Open Source SoC](#)



Jason Kridner

- Jason Kridner is a founder of the [BeagleBoard.org Foundation](https://beagleboard.org) and president of the board. Jason is an independent [embedded systems consultant](#). As a 28 year veteran of Texas Instruments, he developed experience in the design, manufacturing, testing and applications of integrated circuits used in embedded systems
- BeagleBoard.org news: member of [RISC-V International](#) and [OpenHW Group](#); students can apply **now** to [Google Summer of Code](#), join the [open chips forum](#) to discuss plans for open source RTL chip designs, including in FPGAs and in silicon
- **[BeagleV to launch in 2021](#)**: open hardware board designed to run Linux on RISC-V



A quick introduction to FPGAs

- Field Programmable Gate Arrays (FPGA) are an important part of many hardware designs. An FPGA is a chip which can be configured to perform any logic function within the limits of its resources and the ability of the designer.
- The inside of an FPGA can be very loosely described as a “sea” of configurable gates, flip-flops and interconnect. In the old days, designers used chips from e.g. the 7400-series to design a Printed Circuit Board (PCB) which would carry out a given logic function. This was cumbersome and inflexible. A change of functionality often required a modification of the PCB and long delays to wait for manufacturing. With FPGAs, changes in functionality which don't affect the pinout do not need a redesign of the PCB. You just reconfigure the FPGA with an appropriate bitstream.
- The configuration bitstream is the result of applying a set of tools to the design sources, which are typically text files containing Hardware Description Language (HDL) designs.

Note: [FOSSI](#) and [OSHWA](#) are drafting documentation to introduce chip design concepts. Check [@ohsummit](#) for updates.

A quick introduction to HDL and RTL

- When a designer writes HDL code they are not “programming”, but actually “describing” a circuit. This is what the ‘D’ in HDL stands for. Different statements and blocks in HDL describe different parts of a circuit. A piece of circuit does not “happen” before or after another one. They just exist at the same time in different parts of the FPGA silicon. Therefore, we don’t use words like “execute” for a bitstream, because they convey some kind of sequential running of instructions as in software. For similar reasons, some prefer configuring an FPGA (i.e., loading a bitstream) to programming an FPGA, although the latter is very much used as well.
- Some of the HDL you can write is not synthesizable, meaning that there is no clear circuit equivalent to it. These non-synthesizable HDL constructs (for example instructions to read and write from a file) are typically used for writing testbenches, which are used during simulation in a computer. The synthesizable part of HDL is sometimes referred to as RTL (Register Transfer Level) code, although strictly speaking you can write synthesizable HDL which is not RTL.

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Opening Round

- Where in the world are you today?
- Why does open source hardware matter to you?
- What benefit do you think open source development can bring to chip design?